REMARKS

Claims 1, 3-8, and 10-28 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claims 1 and 8 include a limitation for "selecting" "suitable types of test." The Examiner has questioned how these tests are "selected" and where they are selected from. The Examiner suggests that the claims should recite storing a list of tests at some location. Applicants have amended claims 1 and 8 to emphasize that the test types are selected from storage in the repository based on a match between the entered configuration data of the memory model under test and the configuration data of catalogued memory models (having associated test types) from the repository.

Claims 3 and 10 include an antecedent issue. Amendments have been presented to claims 3 and 10 to supply the necessary antecedent.

Claim 8 was further rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps. Applicants have amended claim 8 to include a further "applying" step relating to verification.

The Examiner further objected to the "setting up by" language in claim 8. An amendment to claim 8 is presented to delete the objected to language. See, also, a similar amendment in Claim 1.

In claims 15 and 22, the Examiner notes an issue with respect to how the recited comparing operation can identify tests. Amendments have been presented to claims 15 and 22 to address the claimed tests.

The Examiner further questions how the specific test vectors are generated in accordance with received model data. Claims 15 and 22 have been amended to move the "in accordance with received model data" limitation to a different position in the claim. It is believed that this change in clause position clarifies the limitation.

With respect to claims 19 and 26, the Examiner points out that the antecedent for the repository does not recite the storage of the integrated circuit models. Claims 19 and 26 have been amended to address the noted issue.

Claim 22 includes an antecedent issue. Claim 22 has been amended to address the issue.

In view of the foregoing, Applicants request that the Section 112 rejection of the claims be withdrawn.

Claims 1, 3, 6-8, 10, 13-16, 19, 21-23, 26 and 28 were rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrineh in view of Kebichi. Applicants respectfully traverse the rejection and assert that Zarrineh and Kebichi are not relevant to the claimed invention.

Turning first to Zarrineh, this reference fails to teach storing data (such as catalog data or characteristic data) for integrated circuit models along with a test associated with each circuit model. The Examiner points to the RAM, CAM and FIFO primitives of Zarrineh. The RAM primitive specifies memory structure and operation of the memory if configured as random addressable (page 527, left column, last paragraph). The CAM primitive specifies memory structure and operation of the memory if configured as content addressable (page 527, right column, second to last paragraph). The FIFO primitive specifies memory structure and operation of the memory if configured as RAM addressable with internally handled addresses (page 527, right column, last paragraph). However, there is no specification in the memory primitives of Zarrineh for storing a "test associated with each circuit model."

The Examiner concedes that Zarrineh fails to teach or suggest selecting from the associated/stored tests based on a comparison or matching operation as claimed by Applicants. While the Examiner points to the memory model maker (section 3.3) and the memory block validation (section 4.1) of Zarrineh, it is clear that these teachings are not pertinent to the claimed invention. There is no teaching or suggestion in Zarrineh for comparing or matching as recited in the independent claims so as to select certain ones of the tests. Zarrineh teaches "automatic test pattern generation," and that the "gate-level description of the memory block is first loaded in the test framework and used to generate test patterns and report the fault coverage" (section 4.1). While this would teach generating test patterns, there clearly is no teaching for performing a comparison or matching operation so as to select (from associated storage) tests applicable to a circuit model.

The Examiner further asserts that selecting from the associated/stored tests based on a comparison or matching operation is taught by Kebichi. Applicants respectfully disagree for a number of reasons.

First, Applicants submit that the combination of Kebichi with Zarrineh is improper. A review of Kebichi reveals that this reference is directed to providing instructions to a built-in self test (BIST) of an integrated circuit for purpose of circuit testing. Thus, Kebichi is focused on testing of the actual fabricated integrated circuit itself (i.e., testing the silicon). The testing of an actual integrated circuit for the purposes of finding errors in the silicon fabricated circuit is not the same thing as generating test patterns concerning, and relating to the testing of, a "model" of an integrated circuit. One skilled in the art with knowledge of Zarrineh and working on model testing would have no reason to consider fabricated semiconductor circuit testing (such as BIST) for testing of the model. In fact, there is no teaching or suggestion in Kebichi for extending or using any of Kebichi's BIST teachings to the model testing described in Zarrineh. Likewise, Zarrineh fails to teach or suggest considering use of BIST-like circuit testing procedures in the context of model testing and the automatic test pattern generation tools. The proposed combination of references is thus improper.

The foregoing conclusion is reinforces when one considers the intent of the two testing operations. With respect to BIST-type testing on actual fabricated integrated circuits, the point of the testing is to determine whether a fabrication error has occurred. With respect to model testing, a model of a proposed circuit is defined, and the testing is performed to determine whether the model of the proposed circuit functions in the manner expected by the designer (or in the alternative as taught in section 4.1 of Zarrineh; whether two models are equivalents of each other). Such model testing will not, and cannot, determine whether a fabrication defect in the silicon circuit has occurred. Conversely, BIST-type testing of the silicon circuit will not, and cannot, determine whether a model of the circuit is accurate. BIST relates to testing implemented by the fabricated integrated circuit itself; it is not a model-based testing and it is not clear from either cited reference that the BIST techniques or algorithms could be used in connection with testing a model using test vectors as claimed.

Second, even if the combination of references were proper, which it is not, the combined teaching still fails to reach the limitations of the independent claims. Applicants claim selecting from the associated/stored tests based on a comparison or matching operation. The Examiner points to Kebichi col. 4, lines 1-5 and 13-33. Notably, the Examiner's analysis on page 8 of the office action apparently ignores the comparison and matching limitations present in the claims for choosing model tests. The cited portions of Kebichi teach associating certain algorithms for testing fabricated integrated circuit operation with certain memory models. If the circuit uses the model, then the testing algorithm is utilized in connection with generating the BIST controller HDL description. Again, this relates to testing of the actual fabricated integrated circuit through the BIST process, and not for testing the model itself. This is where the claimed invention is quite distinct from Kebichi because Kebichi is focused on providing the proper BIST process test for the resulting (fabricated) integrated circuit, and is not in any way concerned with the claimed invention where model tests are associated and then selected based on the comparison and matching operations for use in connection with the generation of test vectors for testing the model (not the fabricated integrated circuit).

Lastly, Applicants claim that the "software-based test case file generation algorithm" is executed for the purpose of generating specific test vectors for each of the test which were identified through the comparison and matching operations. These test vectors enable unique testing of the model. Again, this is to be distinguished from testing of the fabricated integrated circuit as in Kebichi. Kebichi is thus irrelevant to this limitation.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

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Respectfully submitted,

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